

MC14013B

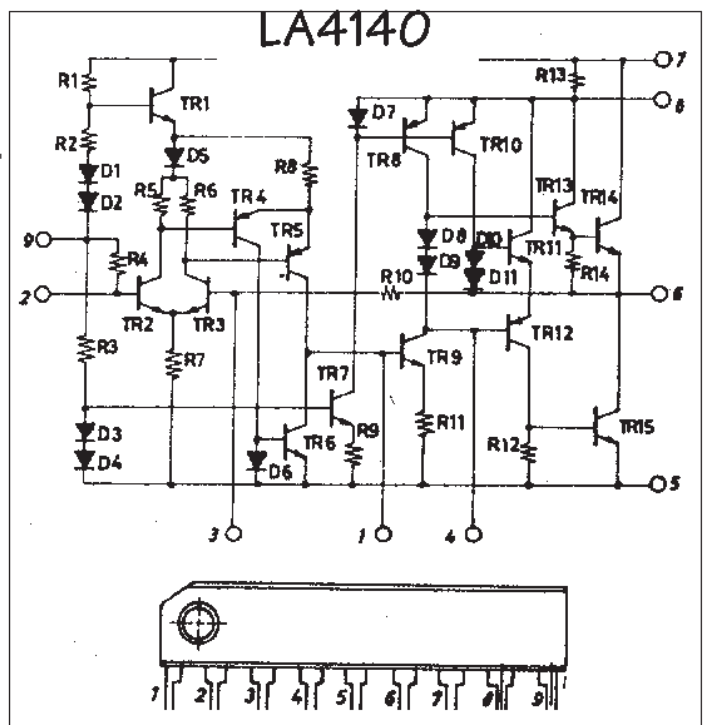
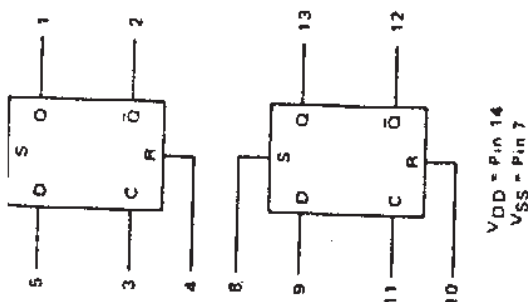
DUAL TYPE D FLIP-FLOP

TRUTH TABLE

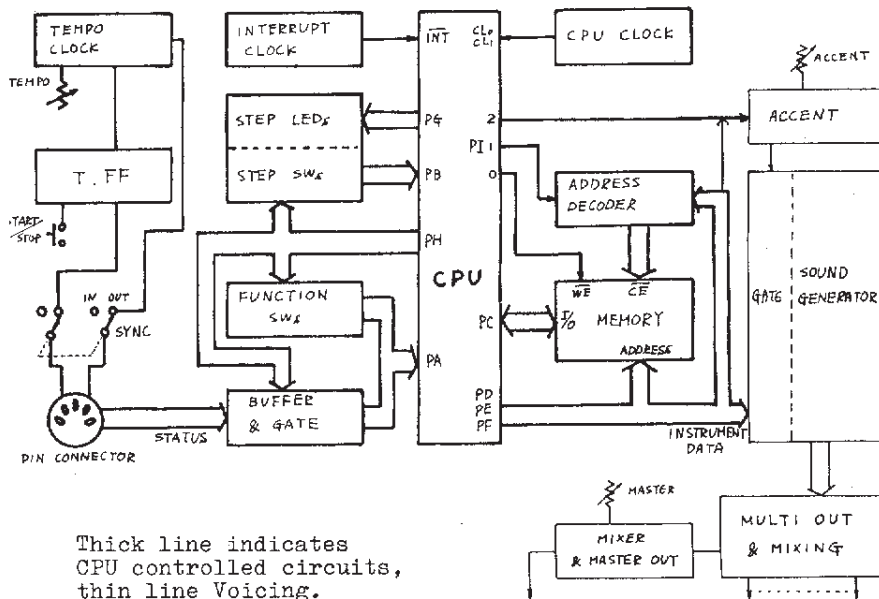
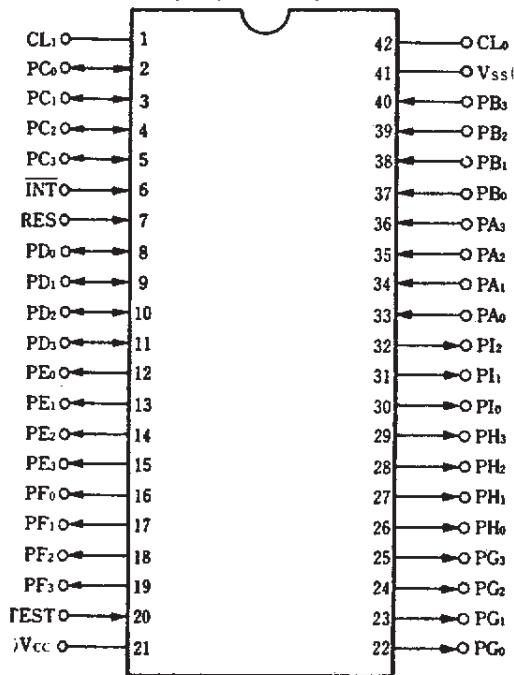
CLOCK ¹	INPUTS			OUTPUTS	
	DATA	RESET	SET	Q	\bar{Q}
	0	0	0	0	1
	1	0	0	1	0
	X	0	0	Q	\bar{Q}
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

No Change

X = Don't Care
1 = Level Change



μPD650C (Top View)



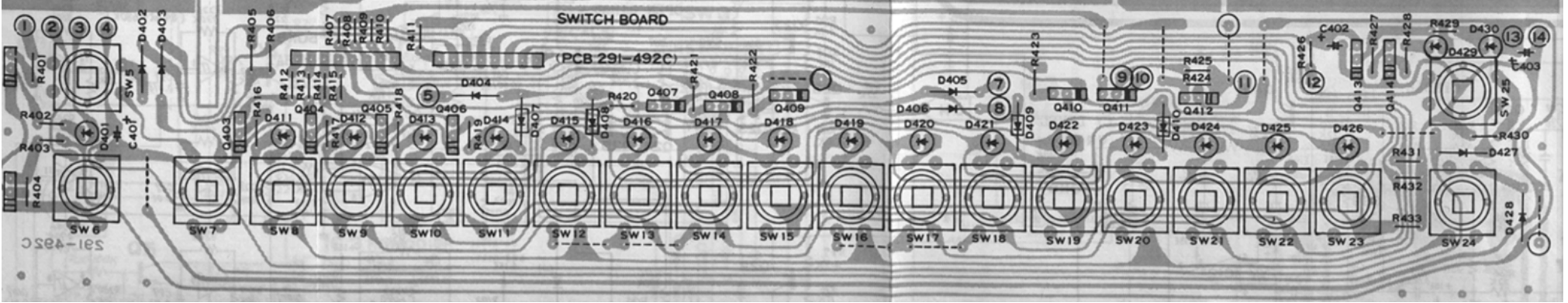
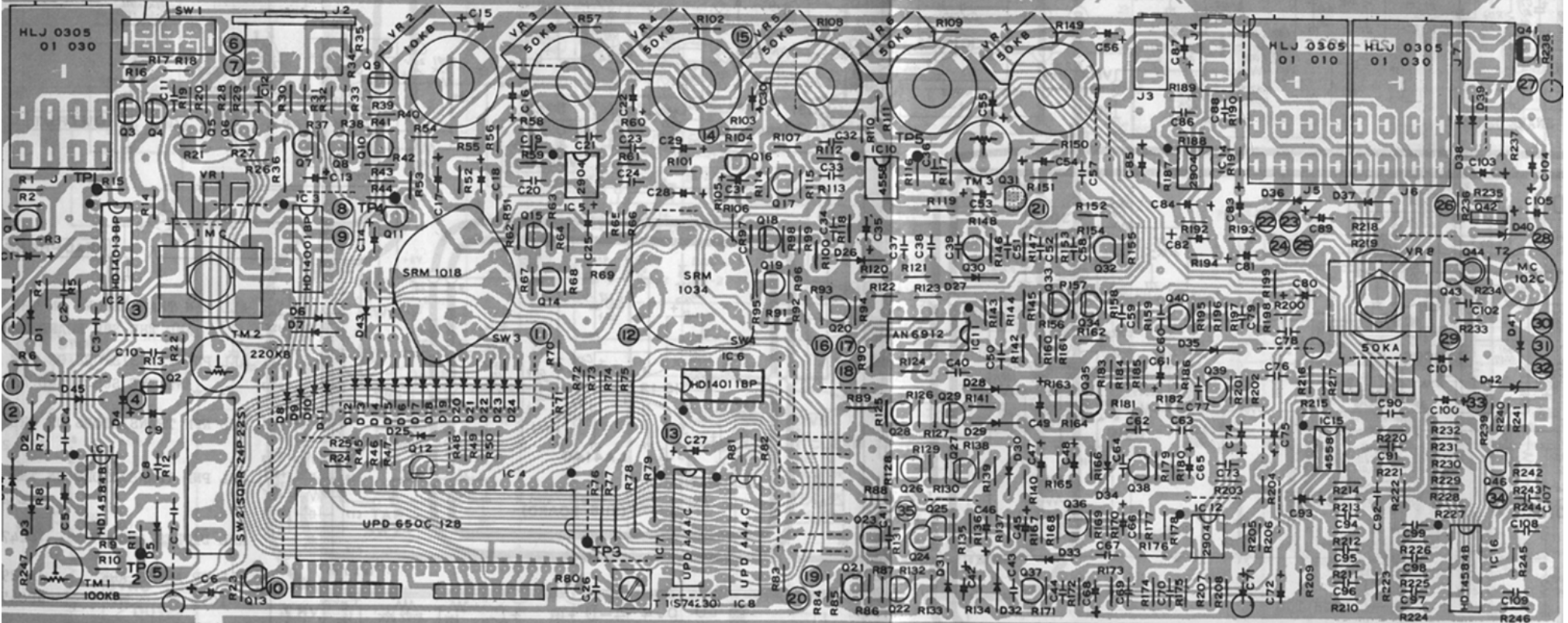
Thick line indicates CPU controlled circuits, thin line Voicing.

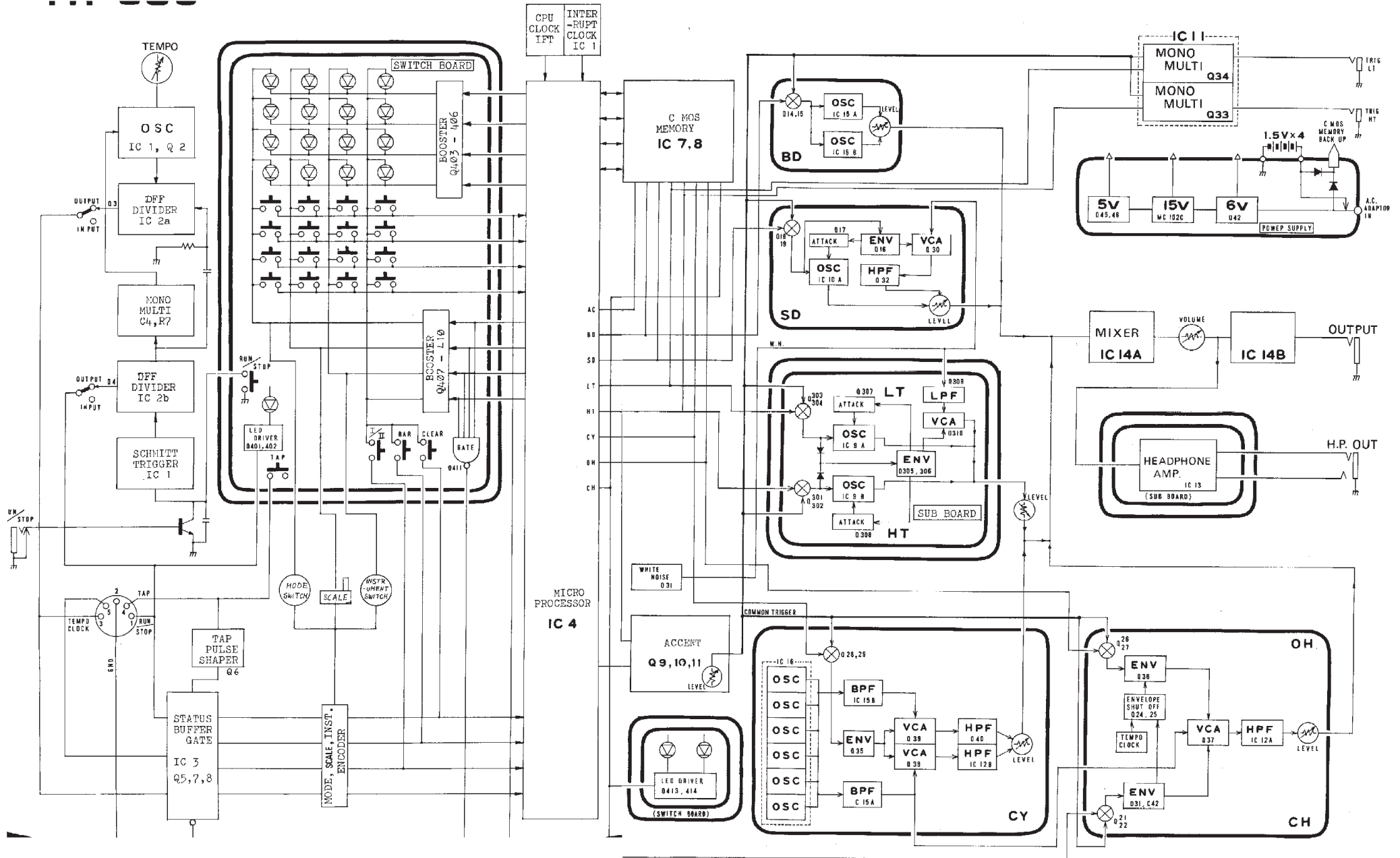
BLOCK DIAGRAM

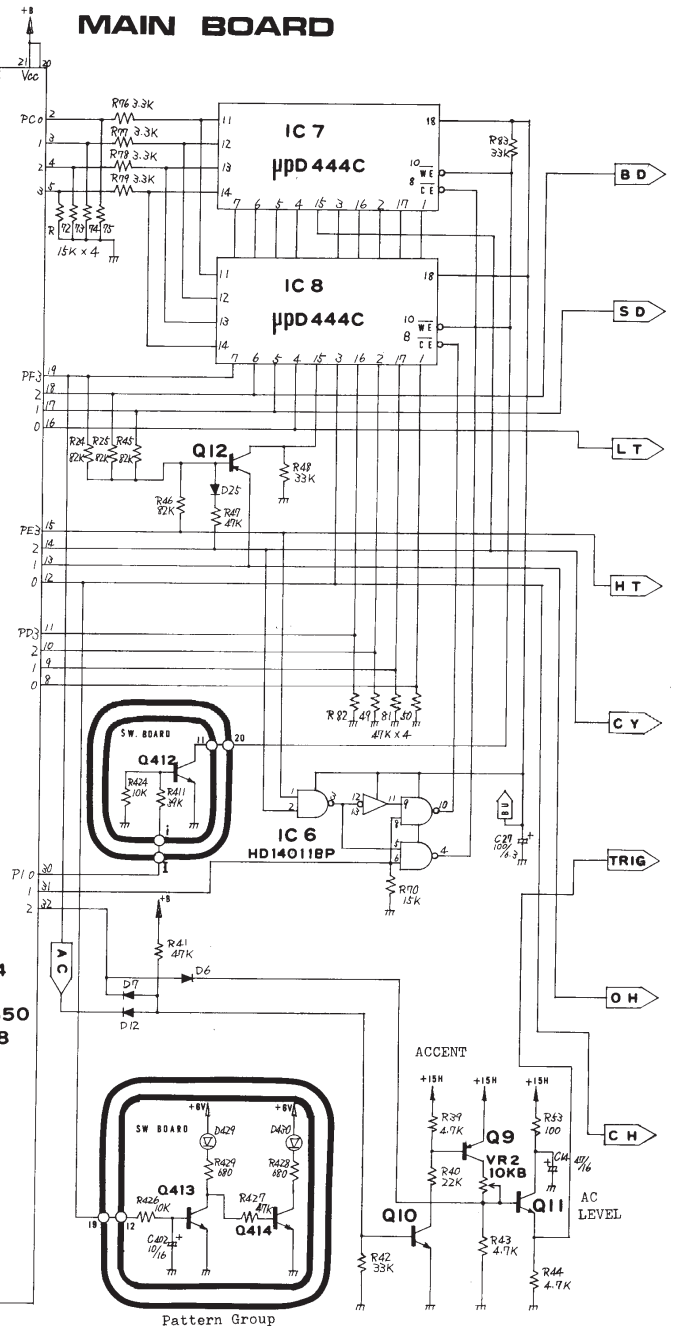
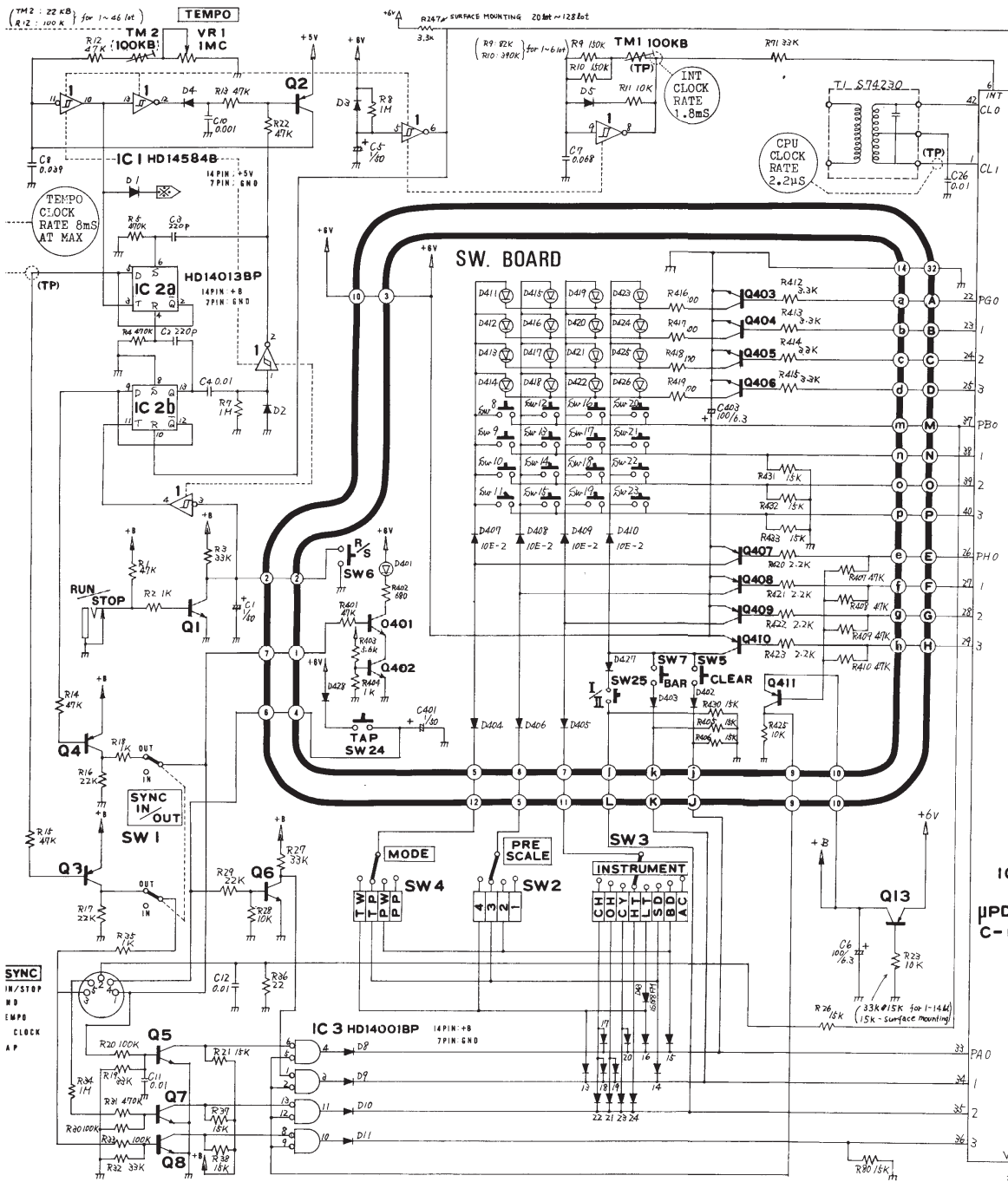
μPD650C-085 FUNCTIONAL DESCRIPTION

No.	Description
PH (Port H) 0 26 1 27 2 28 3 29	Scanning signal outputs to switches Switching signal outputs to STATUS BUFFER & GATE
PA (Port A) 0 33 1 34 2 35 3 36	Switch scanning signal inputs STATUS (TEMPO CLOCK, START/STOP, TAP) inputs
PB (Port B) 0 37 1 38 2 39 3 40	Inputs from STEP Switches (RHYTHM SELECT Switches)
PG (Port G) 0 22 1 23 2 24 3 25	Drive signals to STEP LEDs
PE (Port E) 0 12 1 13 2 14 3 15	I/II Memory bank select CH OH CY HT
PD (Port D) 0 8 1 9 2 10 3 11	MEMORY ADDRESSES These pins use CE from ADDRESS Decoder to select cells in RAM to be accessed INSTRUMENT DATA These data need COMMON TRIG to trigger Sound Generators being designated
PF (Port F) 0 16 1 17 2 18 3 19	LT SD BD AC
PC (Port C) 0 2 1 3 2 4 3 5	Data Inputs/Outputs
PI (Port I) 0 30 1 31 2 32	Memory WE Memory CE (associated with PE-2, 3 at ADDRESS DECODER) Trigger Pulse (INSTRUMENT) output

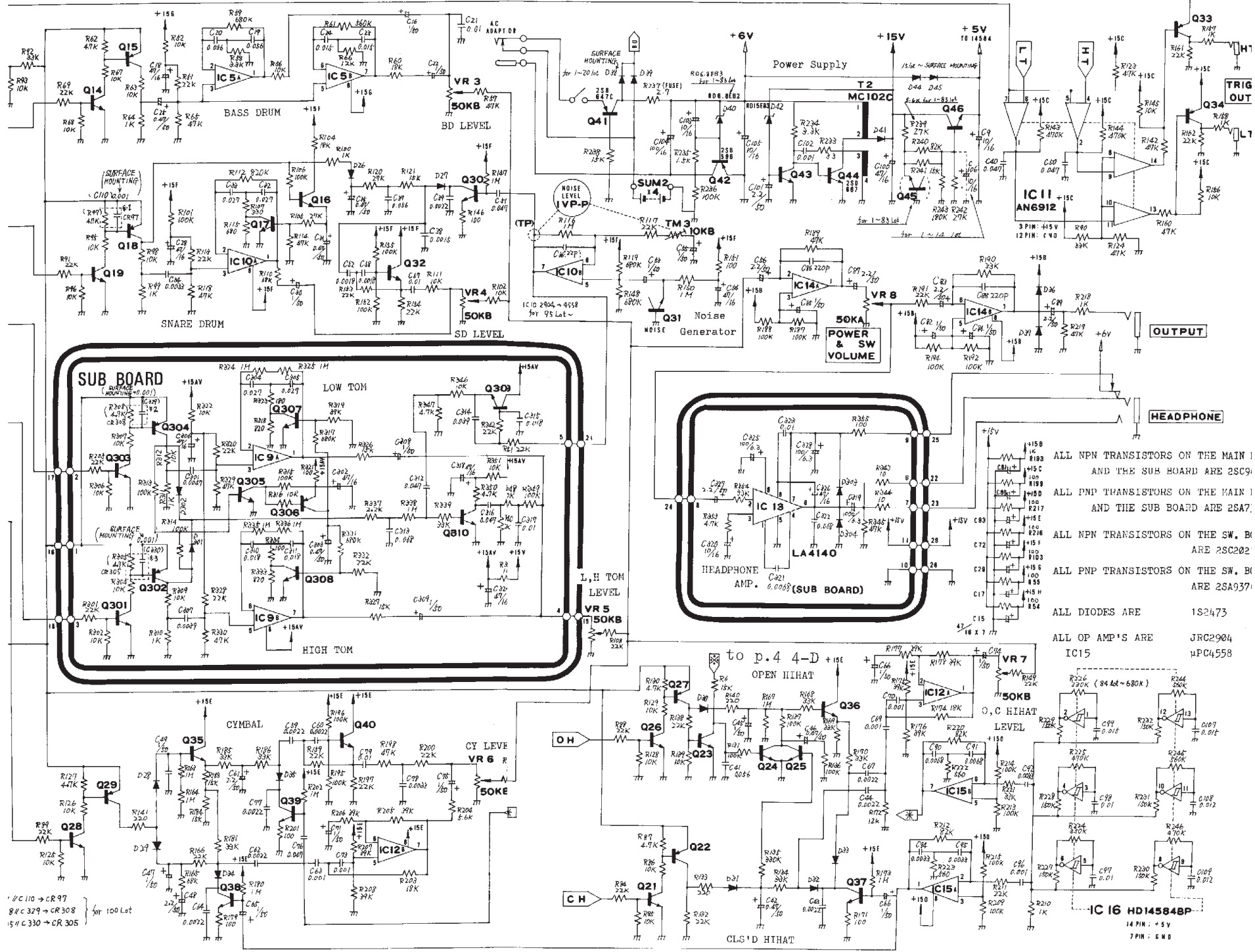
SUB BOARD
581-484C
(PCB 291-494C)







MAIN BOARD



- ALL NPN TRANSISTORS ON THE MAIN BOARD AND THE SUB BOARD ARE 2SC99
- ALL PNP TRANSISTORS ON THE MAIN BOARD AND THE SUB BOARD ARE 2SA7.
- ALL NPN TRANSISTORS ON THE SW. BOARD ARE 2SC202
- ALL PNP TRANSISTORS ON THE SW. BOARD ARE 2SA937.
- ALL DIODES ARE 1S2473
- ALL OP AMP'S ARE JRC2904
- IC15 μPC4558

* IC110 → CR97
 84C329 → CR308
 154C330 → CR305